Session 26 Overview

Cellular Building Blocks and SoCs

Chair: Charles Chien, SST Communications, Marina Del Rey, CA

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Since 1990, we have witnessed a tremendous growth in wireless technology that has positively impacted our daily lives. During the early stages of this wireless revolution, analog cellular and paging technology were widely used. Later these analog systems migrated to digital transmission technology. The so-called second-generation (2G) digital cellular systems include *global system for mobile communications* (GSM), *personal handy-phone system* (PHS), IS95 CDMA, and IS136 TDMA. More recently 2.5G digital cellular systems such as *GSM packet radio system* (GPRS) and 3G cellular systems have emerged to support services for not only voice but also digital images, video streaming, and music downloads. Current penetration of 2G and 2.5G cellular technology has reached a global scale with number of subscribers surpassing 1.5 billion and growing steadily at 7 to 10% every year. One major factor that has spurred this rapid growth is the advent of low-cost semiconductor technology that has made it possible to integrate complex wireless circuits and digital processing on highly integrated low-cost SoCs.

The ten papers in this session represent a snapshot of the recent advances in cellular integrated circuits, ranging from high-performance building blocks to fully integrated cellular SoCs that include both RF/analog and digital processing on the same chip. It is shown in these papers that the continued scaling of silicon technologies can enable increased levels of integration and enhanced performance, while reducing the overall system cost.

Five of the papers in this session cover building blocks for GSM systems. Paper 26.1 describes a highly linear direct-conversion front-end for GSM in 90nm CMOS that achieves 51dBm IIP2. Paper 26.4 presents a 0.25µm CMOS low-IF receiver that achieves greater than 50dB image-rejection ratio based on digital calibration over the entire signal bandwidth at 200kHz IF. Paper 26.5 presents a 0.18µm CMOS fractional-N synthesizer that achieves integrated phase noise of 0.8° using LMS-based DAC gain calibration. Paper 26.9 presents a 0.13µm CMOS power amplifier that is applicable for GSM. With the Doherty topology, it delivers 1.5W at 1.7GHz. Paper 26.10 presents a 65nm $\Delta\Sigma$ modulator that achieves peak SNDRs of 90dB and 62dB for GSM and WCDMA, respectively.

Two papers in this session cover GPS which are becoming an essential component for modern handsets that must support location-based services and E-911. Paper 26.2 describes a 0.13µm CMOS GPS front-end that dissipates only 5.4mW using current-reuse of the LNA, mixer, and VCO. Paper 26.3 describes a fully integrated GPS receiver in 0.18µm SiGe BiCMOS that addresses the coexistence of GPS with cellular transmissions.

Paper 26.6 presents a 90nm CMOS software-defined radio receiver that covers various bands in the 800MHz to 5GHz frequency range. The tuning over multiple RF bands and 100dB dynamic range are achieved with 5 to 5.5dB of NF, -3.5dBm of IIP3, and 39dBm of IIP2. This radio can receive signals for various standards such as GSM and IEEE 802.11b/g.

Finally, two papers in this session cover cellular SoCs which include not only the RF/analog circuits but also digital processing on the same chip. Paper 26.7 presents the first true SoC for quad-band GSM/GPRS that integrates RF, analog/mixed signal blocks, digital signal processing, application processor, RAM/ROM, and audio circuitry. This SoC is implemented in a low-cost 0.13µm CMOS process, while achieving a sensitivity of less than -110dBm and a transmit power of greater than 3dBm.

Paper 26.8 presents the first SoC for PHS system that include all RF, analog baseband, power management, and digital functions of a handset. This SoC is implemented in a low-cost 0.18µm CMOS process. It draws 81mA from a 1.8V supply, occupies 35mm^2, and achieves -106dBm sensitivity, +4dBm EVM-compliant transmit power, and 15µs synthesizer settling time.

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26.1 **A 750mV 15kHz 1/f Noise Corner 51dBm IIP2 Direct-Conversion Front-End for GSM in 90nm CMOS** **8:30 AM**
M. Brandolini, Università degli Studi di Pavia, Pavia, Italy

A direct-conversion front-end using a highly linear mixer is implemented in 90nm CMOS. The front-end shows 15kHz 1/f noise corner, 51dBm IIP2, 31.5dB gain, 3.5dB NF, and draws 15mA from 0.75 V.

26.2 **A 5.4mW GPS CMOS Quadrature Front-End Based on a Single-Stage LNA-Mixer-VCO** **8:45 AM**
A. Liscidini, Università degli Studi di Pavia, Pavia, Italy

A GPS RF front-end combines the LNA, mixer, and VCO in a single stage and can operate from a 1.2V supply. The chip is implemented in a 0.13µm CMOS process and occupies 1.5mm^2 active area. It consumes 5.4mW with a 4.8dB NF, 36dB gain, and a P_{1dB} of -31dBm.

26.3 **A 20mW 3.24mm^2 Fully Integrated GPS Radio for Cell-Phones** **9:00 AM**
V. Della Torre, RFDomus, Newport Beach, CA

A GPS receiver that can coexist with cellular transceivers is implemented in a 0.18µm SiGe BiCMOS technology and occupies 3.24mm^2. The device integrates polyphase filters, VGA, ADCs, fractional-N synthesizer, LNA, and mixers, minimizing desensitization and reciprocal mixing. The receiver consumes 20mW from a 1.8V supply and has 1dB gain desensitization with a -8dBm 1.9GHz blocker

26.4 **Wideband Image-Rejection Circuit for Low-IF Receivers** **9:30 AM**
K. Maeda, Hitachi, Tokyo, Japan

A wideband image-rejection circuit for GSM/EDGE low-IF receivers includes a reference signal source and digital correction circuit that compensate I/Q gain, phase, and frequency response mismatch. The chip integrates an LNA, mixers, PGAs, LPFs, and fractional-N synthesizer in a 0.25µm BiCMOS process and achieves 50dB IRR over the entire signal bandwidth at 200kHz IF.

26.5 **A 1.8GHz Spur-Cancelled Fractional-N Frequency Synthesizer with LMS-Based DAC Gain Calibration** **9:45 AM**
M. Gupta, University of California, San Diego, CA

A 1.8GHz wideband fractional-N synthesizer achieves the phase noise of an integer-N PLL using a noise-cancellation DAC calibrated with an adaptive LMS spur correlation technique. It exhibits in-band and integrated phase noises of -98dBc/Hz and 0.8°, respectively. The chip in 0.18µm CMOS occupies 2mm^2, and consumes 29mW at 1.8V.

26.6 **An 800MHz to 5GHz Software-Defined Radio Receiver in 90nm CMOS** **10:15 AM**
R. Bagheri, University of California, Los Angeles, CA and WiLinx, Los Angeles, CA

A 90nm CMOS RX operates over the 800MHz to 5GHz band uses a passive FET mixer driven by a capacitively coupled RF transconductor, and a combination of CT and DT analog FIR and IIR filters to achieve >100dB of programmable anti-aliasing. The RX chain has 5 to 5.5dB NF, -3.5dBm IIP3, 39dBm IIP2, 10 to 66dB of gain, and draws 11.4mA from 2.5V and 8 to 28mA (depending on RX mode) from 1V.

26.7 **A Fully Integrated SoC for GSM/GPRS in 0.13µm CMOS** **10:45 AM**
J. Kissing, Infineon, Sophia Antipolis, France

A single-chip radio for quad-band GSM/GPRS applications integrates the RF, analog/mixed-signal blocks, DSP, application processor, RAM/ROM, and audio. It is implemented in a 0.13µm CMOS process. The RX achieves -112.5dBm/-110.5dBm sensitivity and the TX meets all the spectral mask requirements while using a 1.5V supply.

26.8 **A 1.9GHz Single-chip CMOS PHS Cellphone** **11:15 AM**
W. Si, Atheros, Santa Clara, CA

A single-chip CMOS PHS cellphone, fabricated in a 0.18µm CMOS process, implements all handset functions including radio, voice, audio, CPU, and digital interfaces. The IC has +4dBm EVM-compliant transmit power, -106dBm receiver sensitivity, and 15µs synthesizer settling time. It draws 81mA from a 1.8V supply while occupying 35mm^2 of chip area.

26.9 **A 1.7GHz 1.5W CMOS RF Doherty Power Amplifier for Wireless Communications** **11:45 AM**
N. Wongkomet, University of California, Berkeley, CA

A fully differential Doherty PA is implemented in 0.13µm CMOS with MIM capacitors and a die size of 2.8×3.2mm^2. The prototype achieves a maximum output power of 1.5W at 1.7GHz with a drain efficiency of 39%. The peak PAE is 36% (33% with off-chip balun) including the driving stages and is >18% for a 10dB range of output power.

26.10 **A 1.2V Dual-Mode GSM/WCDMA ΔΣ ADC in 65nm CMOS** **12:00 PM**
J. Järvinen, Helsinki University of Technology, Espoo, Finland

A dual-mode ΔΣ ADC for a GSM/WCDMA direct-conversion receiver is implemented in a standard 65nm digital CMOS process and has a core area of 0.1mm^2. With sampling frequencies of 48MHz and 96MHz, the ADC achieves peak SNDRs of 84dB and 49dB over the 100kHz GSM band and 1.92MHz WCDMA band, respectively. It draws 2.75mA in GSM mode and 3mA in WCDMA mode from a 1.2V supply.